1. (original) A HDD, comprising:

at least one write channel including at least one write gate; and

control circuitry encoding write control bits for controlling the write gate to selectively enable writing data bits associated with a servo pattern onto at least one disk.

2. (original) The HDD of Claim 1, wherein the write channel is used during operation to write user data to the disk.

3. (original) The HDD of Claim 1, wherein the control circuitry encodes two bits of a ten bit parallel bus to indicate whether the write gate should enable writing one or more of the remaining eight bits of the bus to disk.

4. (original) The HDD of Claim 1, wherein the control circuitry encodes four bits of an eight bit parallel bus to indicate whether the write gate should enable writing one or more of the remaining four bits of the bus to disk.

5. (original) The HDD of Claim 2, wherein the control circuitry determines a write delay to a next timing mark based on a current timing mark, the time delay including a clock cycle component and a clock phase component, the write channel using the write delay to write the next timing mark and associated portions of the servo pattern to disk.

6. (original) A method for self-writing a servo pattern to a disk using a write channel intended for subsequently writing user data, comprising:

receiving a servo pattern defined by a stream of data bits; and

associating write control bits with the servo pattern, values of the write control bits indicating whether a write gate associated with the write channel is enabled or disabled.

7. (original) The method of Claim 6, wherein a write control bit is associated with at least one data bit.

8. (original) The method of Claim 7, wherein a write control bit is associated with one and only one data bit.

9. (original) The method of Claim 7, wherein a write control bit is associated with at least two data bits.

10. (original) The method of Claim 6, comprising writing the servo pattern on the disk after the disk has been sealed in a housing.

11. (original) The method of Claim 6, further comprising:

determining a write delay to a next timing mark based on detecting a current timing mark, the time delay including a clock cycle component and a clock phase component; and

using the write delay to write the next timing mark and associated portions of the servo pattern to disk.

12. (original) A system, comprising:

a hard disk drive controller;

at least one disk onto which the controller writes user data using at least one write channel, the write channel including a write gate; and

means for, at least prior to providing the system to the user, generating gate control means for selectively enabling and disabling the write gate while the write channel remains energized to write a servo pattern on the disk.

13. (original) The system of Claim 12, wherein the gate control means include write control bits.

14. (original) The system of Claim 13, wherein two write control bits of a ten bit parallel bus establish write control bits to indicate whether the write gate should enable writing one or more of the remaining eight bits of the bus to disk.

15. (original) The system of Claim 13, wherein four bits of an eight bit parallel bus establish write control bits to indicate whether the write gate should enable writing one or more of the remaining four bits of the bus to disk.

16. (original) The system of Claim 12, comprising control circuitry determining a write delay to a next timing mark based on detecting a current timing mark, the time delay including a clock cycle component and a clock phase component, the write channel using the write delay to write the next timing mark and associated portions of the servo pattern to disk.

17. (currently amended) A HDD, comprising:

at least one write channel configured for writing user data to a disk; ~~and~~

control circuitry determining a single write delay from a prior timing mark to indicate writing of a subsequent timing mark and at least a portion of a servo pattern; and

at least one write gate in the write channel, the write gate being controllable using write control bits generated by the control circuitry to selectively enable writing data bits associated with a servo pattern onto at least one disk.

18 (canceled).